FEATURES

- 8M-bit Serial Flash
  - -8M-bit/1024K-byte
  - -256 bytes per programmable page

- Software/Hardware Write Protection
  - -Write protect all/portion of memory via software
  - -Enable/Disable protection with WP# Pin

- High Speed Clock Frequency
  - -150MHz for fast read with 30PF load
  - -100MHz for normal read with 30PF load
  - -100MHz for Dual data I/O mode

- Flexible Architecture
  - -256 sectors of 4K-byte
  - -16 blocks of 64K-byte
  - -blocks and sectors are erasable individually

- Low Power Consumption
  - -20mA maximum active current
  - -5uA maximum power-down current

- Program/Erase Speed
  - -Page Program time: 1.5ms typical
  - -Sector Erase time: 300ms typical
  - -Block Erase time: 800ms typical
  - -Chip Erase time: 10s typical

- Single Power Supply Voltage
  - -Full voltage range: 2.7~3.6V

- Lockable 256-byte OTP Security Sector

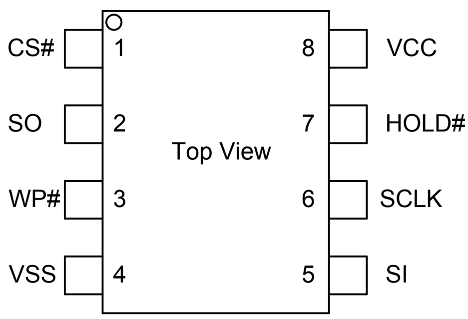
- Minimum 100,000 Program/Erase Cycles

GENERAL DESCRIPTION

The GD25T80 is a 8,388,608 bit Serial Flash Memory, with advance write protection mechanisms, accessed by a high speed SPI-compatible bus: a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the Memory is enabled by CS# input.

The GD25T80 is designed to allow sector erase, block erase and chip erase operation. The device can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100,000 program/erase cycles.

CONNECTION DIAGRAM

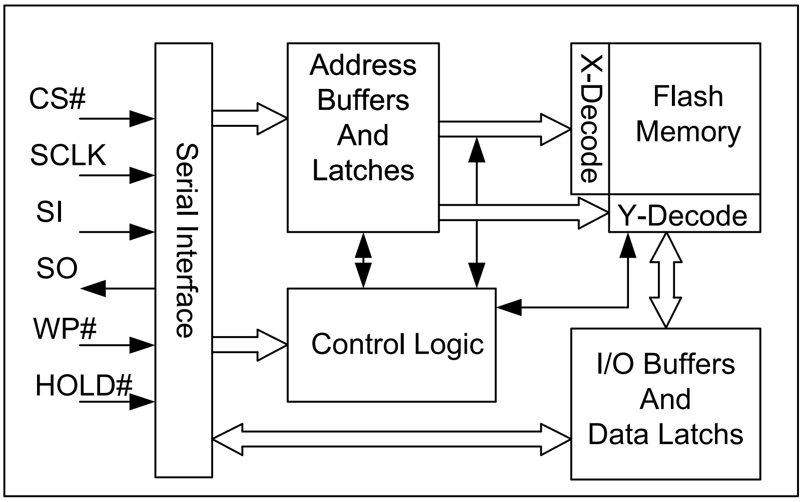


8－LEAD SOP

PIN DESCRIPTION

Pin	I/O	Description
CS#	**Input**	**Chip Select (CS#):** The SPI Chip Select (CS#) Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written. Device is in stand-by mode when a program, erase, or Write Status Register operation is not in progress.
SO	**Output**	**Serial Data Output (SO):** The SPI Serial Data Output (SO) transfer data serially out of the device on the falling edge of SCLK.
WP#	**Input**	**Write Protect (WP#):** The Write Protect (WP#) protect the memory area specified by status register protect bit BP0~BP2.
SI	**Input**	**Serial Data Input (SI):** The SPI Serial Data Input (SI) transfer data serially into the device, the device latch commands, addresses and data on the rising edge of SCLK.
SCLK	**Input**	**Serial Clock (SCLK):** The SPI Serial Clock Input (SCLK) pin provides the timing for serial input and output operations.
HOLD#	**Input**	**Hold (HOLD#):** The HOLD to pause any communication with the device without deselecting it, when it drive low and CS# is low, SO is at high impedance, and input at SI and SCLK are ignored.
VSS	**Input**	Ground
VCC	**Input**	Supply Voltage

BLOCK DIAGRAM



MEMORY ORGANIZATION

Each device has	Each block has	Each sector has	Each page has	
1M	64K	4K	256	bytes
4K	256	16	-	pages
256	16	-	-	sectors
16	-	-	-	blocks

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

UNIFORM BLOCK SECTOR ARCHITECTURE

Block	Sector	Address range	
	255	0FF000h	0FFFFFh
15	……	……	……
	240	0F0000h	0F0FFFh
	239	0EF000h	0EFFFFh
14	……	……	……
	224	0E0000h	0E0FFFh
	223	0DF000h	0DFFFFh
13	……	……	……
	208	0D0000h	0DFFFFh
	……	……	……
……	……	……	……
	……	……	……
	47	02F000h	02FFFFh
2	……	……	……
	32	020000h	02FFFFh
	31	01F000h	01FFFFh
1	……	……	……
	16	010000h	010FFFh
	15	00F000h	00FFFFh
	14	00E000h	00EFFFh
	13	00D000h	00DFFFh
0	……	……	……
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

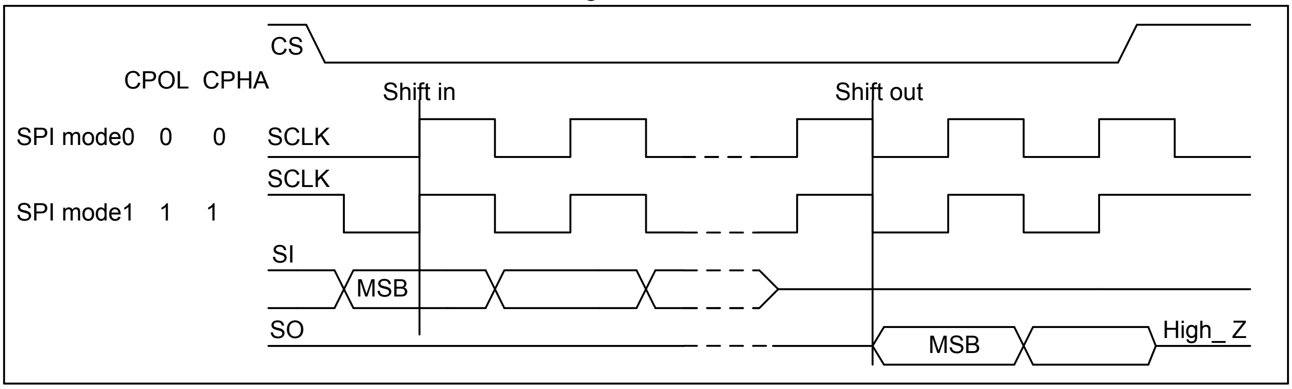
DEVICE OPERATION

SPI Mode

The GD25T80 feature a serial peripheral interface on 4-signal bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported.

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK. The difference of SPI mode 0 and mode 3 is shown as Figure 1.

Figure1. SPI Modes



NOTE:

CPOL indicates clock polarity of SPI master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which SPI mode is supported.

Data Protection

The GD25T80 provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-up
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE)
  -Block Erase (BE)
  -Chip Erase (CE)
- Software Protection Mode (SPM): The Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode (HPM): WP# going low to protected the BP0~BP2 bits and SRP bit.
- Deep Power-down Mode: In Deep Power-down mode, all commands are ignored except the Release from Deep Power-down Mode command.

Table1. Protected area size

Status Register Content			Memory Content			
BP2	**BP1**	**BP0**	**Protect Blocks**	**Addresses**	**Density(KB)**	**Portion**
1	1	1	All	000000h-0FFFFFh	1024K bytes	All
1	1	0	All	000000h-0FFFFFh	1024K bytes	All
1	0	1	All	000000h-0FFFFFh	1024K bytes	All
1	0	0	8 to 15	080000h-0FFFFFh	512K bytes	Upper 1/2
0	1	1	12 to 15	0C0000h-0FFFFFh	256K bytes	Upper 1/4
0	1	0	14 to 15	0E0000h-0FFFFFh	128K bytes	Upper 1/8
0	0	1	15	0F0000h-0FFFFFh	64K bytes	Upper 1/16
0	0	0	None	None	None	None

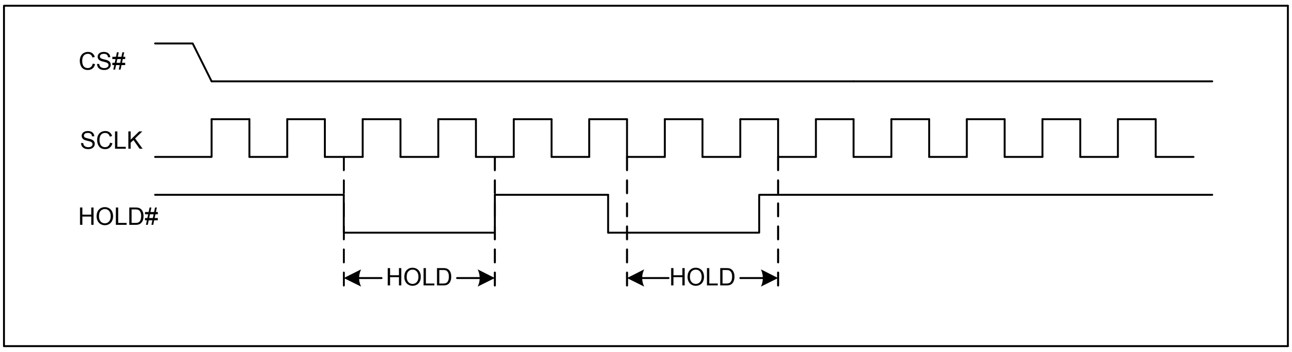
Hold Feature

The Hold (HOLD#) signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD , need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low; (if SCLK is not being low, HOLD operation will not start until SCLK being low) The HOLD condition ends on rising edge of HOLD# signal with SCLK being low. (If SCLK is not being low, HOLD operation will not end until SCLK being low) see Figure 2.

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure2. Hold Condition



Dual SPI mode

(Command/Address/Data all transmitting with 2-bit)

Command	Dual SPI Mode	Command	Dual SPI Mode
Write Enable (06Hex)	√	Block Erase (D8Hex)	×
Write Disable (04Hex)	√	Chip Erase (C7Hex)	×
Read Status Register (05Hex)	√	Deep Power-down (B9Hex)	√
Write Status Register (01Hex)	×	Release from Deep Power-down (ABHex)	√
Read (03Hex)	×	Manufacturer/ Device ID (90Hex)	√
Fast Read (0BHex)	√	Read Identification (9FHex)	√
Dual Output Fast Read (3BHex)	×	Enter EXT Mode (0AHex)	×
Page Program (02Hex)	×	Enter OTP Mode (3AHex)	√
Sector Erase (20Hex)	×		

NOTE: The command with "×" means ignored in Dual SPI Mode.

COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06 Hex						
Write Disable Exit EXT/OTP	04 Hex						
Read Status Register	05 Hex	(S7-S0)					(continuous)
Write Status Register	01 Hex	(S7-S0)					
Read Data	03 Hex	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0B Hex	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Page Program	02 Hex	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	
Sector Erase	20 Hex	A23-A16	A15-A8	A7-A0			
Block Erase	D8/ 52 Hex	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/ 60 Hex						
Deep Power-down	B9 Hex						
Release from Deep Power-down, and read Device ID	AB Hex	dummy	dummy	dummy	(ID7-ID0)		(continuous)
Release from Deep Power-down	AB Hex						
Manufacturer/ Device ID	90 Hex	dummy	dummy	00H	(M7-M0)	(ID7-ID0)	(continuous)
Read Identification	9F Hex	(M7-M0)	(ID15-ID8)	(ID7-ID0)			(continuous)
Enter EXT Mode	0A Hex						
Enter OTP Mode	3A Hex						

NOTE:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the SO pin.
2. When Release from Deep Power-down, and read Device ID. The Device ID will repeat continuously until CS# terminates the command.
3. When Read Manufacturer/ Device ID. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminate the command. 00H on Byte 4 starts with MID and alternate with DID, 01H on Byte 4 starts with DID and alternate with MID.

Table of ID Definitions:

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FHex	C8	31	14
90Hex	C8		13
ABHex			13

Write Enable (WREN) (06Hex)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. (See Figure 3 and Figure 3.1)

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure3. Write Enable Sequence Diagram

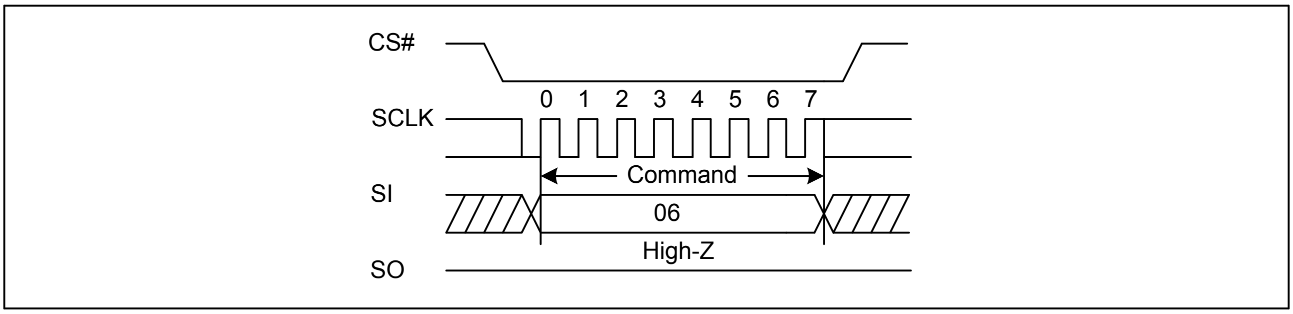
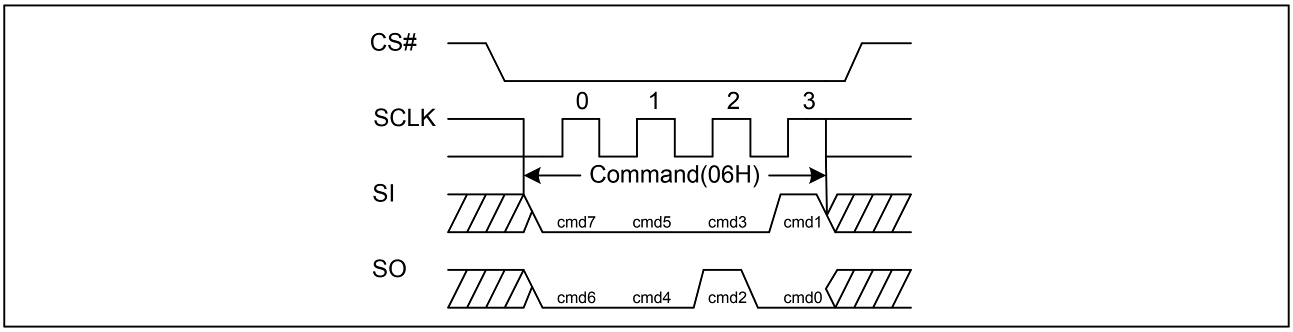


Figure3.1 Write Enable Sequence Diagram of Dual SPI mode



Write Disable (WRDI) (04Hex)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit or exit from EXT/OTP mode to normal mode. The Write Disable command sequence: CS# goes low → Sending the Write Disable command →CS# goes high. (See Figure 4 and Figure 4.1)

The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands

Figure4. Write Disable Sequence Diagram

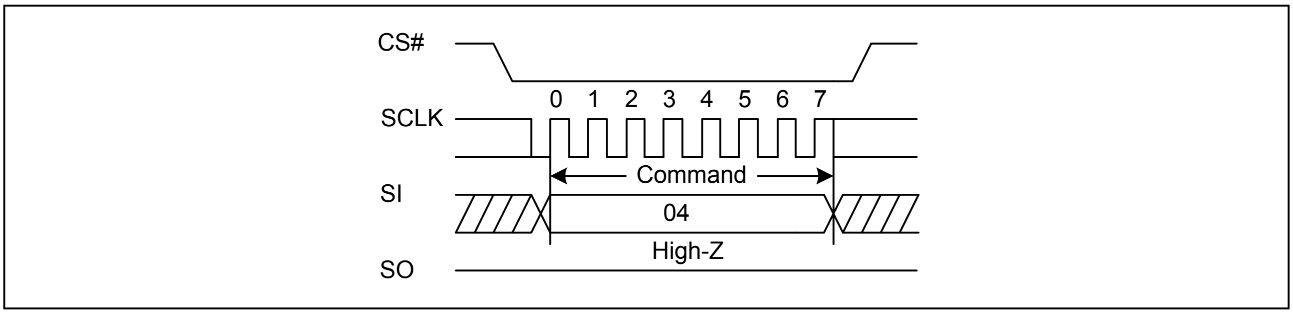
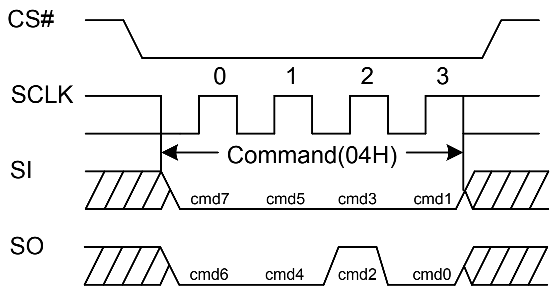


Figure4.1 Write Disable Sequence Diagram of Dual SPI mode



Read Status Register (RDSR) (05Hex)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously.

The Read Status Register command sequence: CS# goes low → Sending Read Status Register command → CS# goes high. (See Figure 5 and Figure 5.1)

Table3. Status Register Bit Location

S7	S6	S5	S4	S3	S2	S1	S0
SRP/ OTP_LOCK	**Mode1**	**Mode0**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**

NOTE: SRP, BP2, BP1 and BP0 are nonvolatile while Mode1, Mode0, WEL and WIP are volatile.

The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress; when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 1) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), commands. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed if, and only if, both Block Protect (BP2, BP1, BP0) bits are 0.

Mode1, Mode0 bits. Default value is SPI Mode (00). Change this value by change mode command to change the interface mode, the device also support Dual SPI mode (01).

SRP bit/OTP_LOCK bit. The Status Register Protect (SRP) bit is operated with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) command is no longer accepted for execution.

In OTP mode the bit is served as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK value is 0, after OTP_LOCK bit is programmed 1 by WRSR command. The OTP sector is protected from program and erase operation. This bit can only be programmed once.

Note: In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Figure5. Read Status Register Sequence Diagram

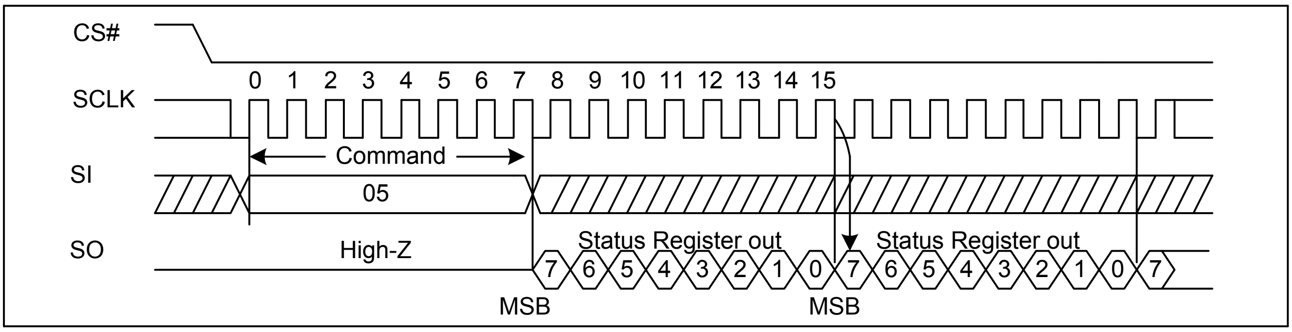
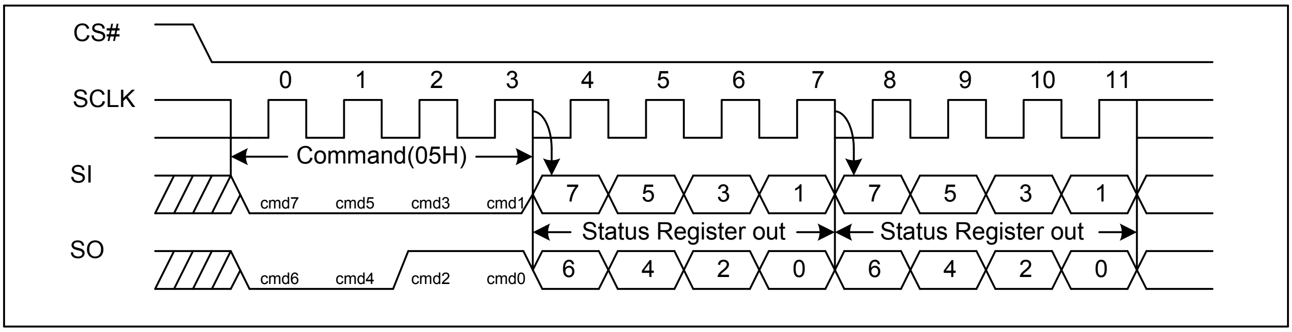


Figure5.1 Read Status Register Sequence Diagram of Dual SPI mode



Write Status Register (WRSR) (01Hex)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command sequence: CS# low → sending Write Status Register command → Status Register data on SI → CS# goes high. (see Figure 6)

The Write Status Register (WRSR) command has no effect on S6, S5, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1.

The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode (HPM) is entered.

Software Protected Mode (SPM):

-When SRP bit=0, no matter WP# is low or high, the WREN command may set the WEL bit and can change the values of SRP,BP2,BP1,BP0. The protected area, which is defined by BP2.BP1.BP0, is at software protected mode (SPM).

-When SRP bit=1 and WP# is high, the WREN command may set the WEL bit can change the values of SRP.BP2.BP1.BP0. The protected area, which is defined by BP2.BP1.BP0, is at software protected mode (SPM).

Note: If SRP bit =1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

-When SRP bit =1, and the WP# is low (or WP# is low before SRP bit =1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP2.BP1.BP0 and hardware protected mode by the WP# to against data modification.

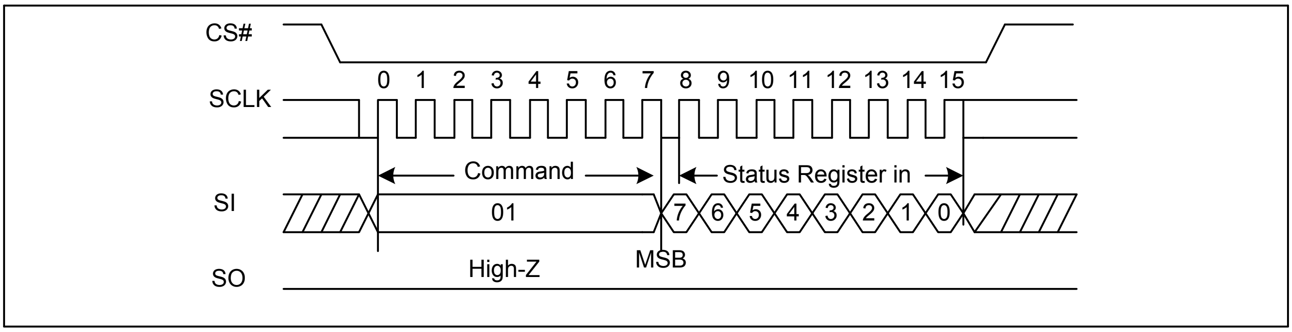
Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered, only can use software protected mode via BP2.BP1.BP0.

Table4. Protection Modes

Mode	Status register condition	WP# and SRP bit status	Memory
Software protection mode(SPM)	Status register can be Written in (WEL bit is set to 1) and the SRP BP0-BP2 bits can be change	WP#=1 and SRP bit =0 or WP#=0 and SRP bit =0 or WP#=1 and SRP bit =1	The protected area cannot be program or erase
Hardware protection mode(HPM)	The SRP,BP0-BP2 of Status Register bits cannot be change	WP#=0,SRP bit =1	The protected area cannot be program or erase

As the above table showing, the summary of the Software Protected Mode (SPM) and hardware Protected Mode (HPM)

Figure6. Write Status Register Sequence Diagram



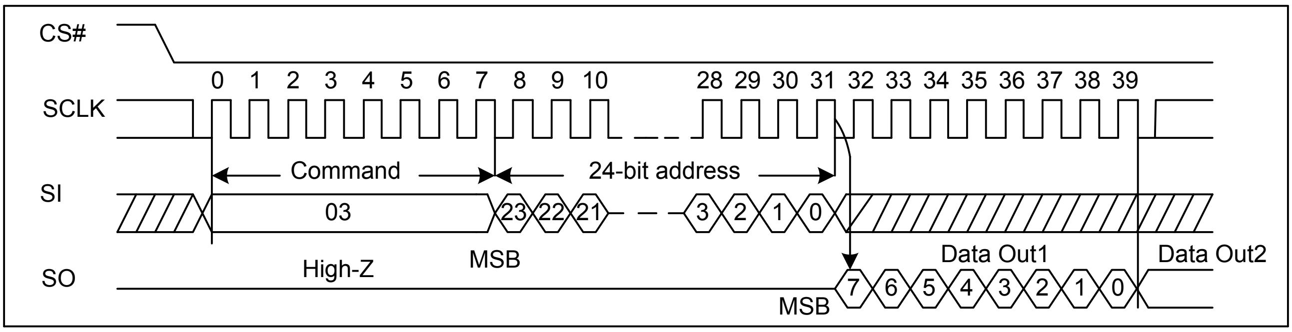
Read Data Bytes (READ) (03Hex)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, during the falling edge of SCLK.

The command sequence is shown in Figure 7. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. When the highest address is reached, the address counter rolls over to 000000H, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) command sequence: CS# goes low → sending READ command → 3-byte address on SI → data out on SO → CS# goes high to end READ. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure7. Read Data Bytes Sequence Diagram



Read Data Bytes at Higher Speed (Fast Read) (0BHex)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK.

The command sequence is shown in Figure 8 and Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (Fast Read) command. When the highest address is reached, the address counter rolls over to 000000H, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (Fast Read) command sequence: CS# goes low → sending Fast Read command → 3-byte address on SI → 1 dummy byte address on SI → data out on SO → CS# goes high to end Fast Read. Any Read Data Bytes at Higher Speed (Fast Read) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress

Figure8. Read Data Bytes at Higher Speed Sequence Diagram

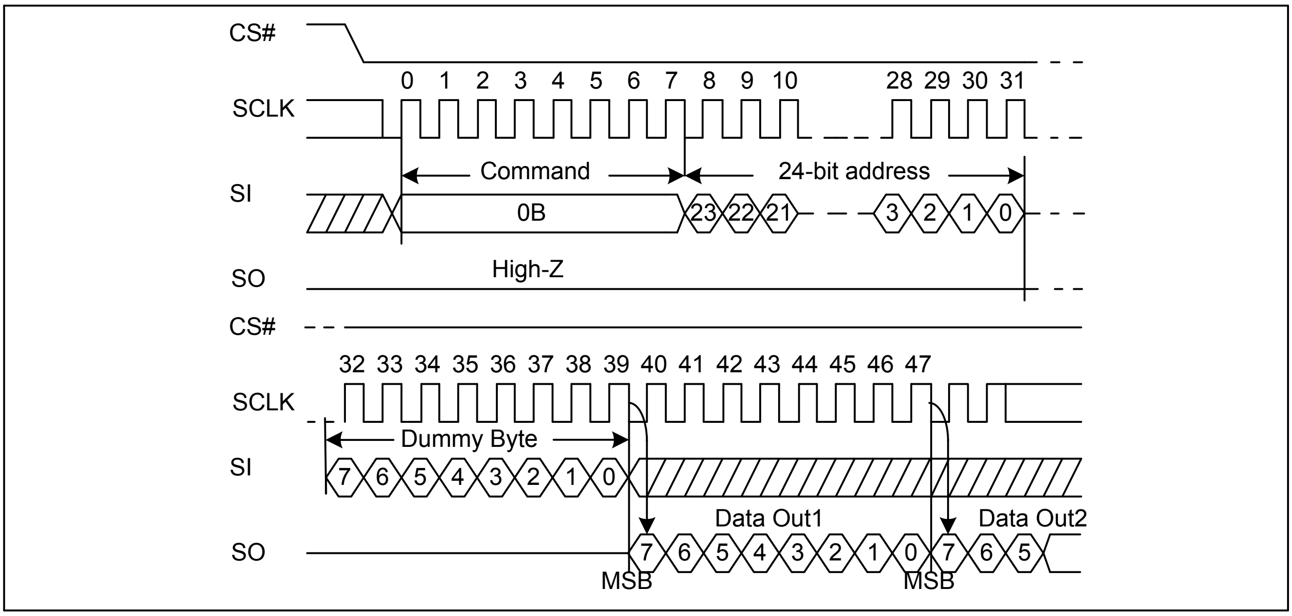
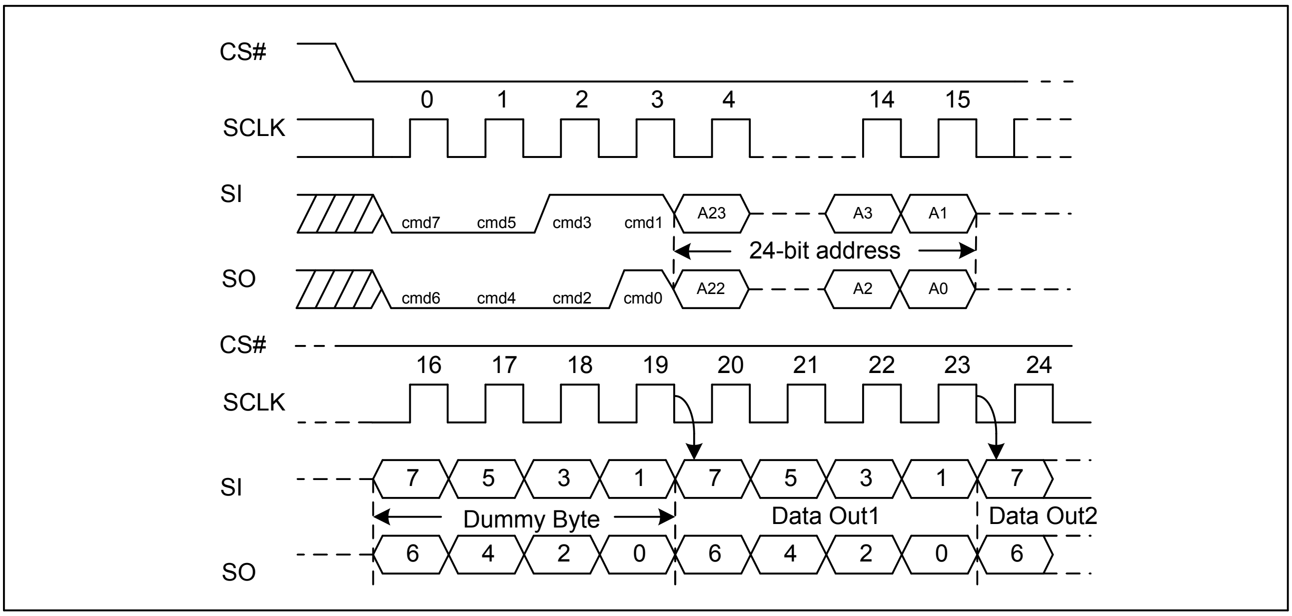


Figure9. Read Data Bytes at Higher Speed Sequence Diagram of Dual SPI mode



Page Program (PP) (02Hex)

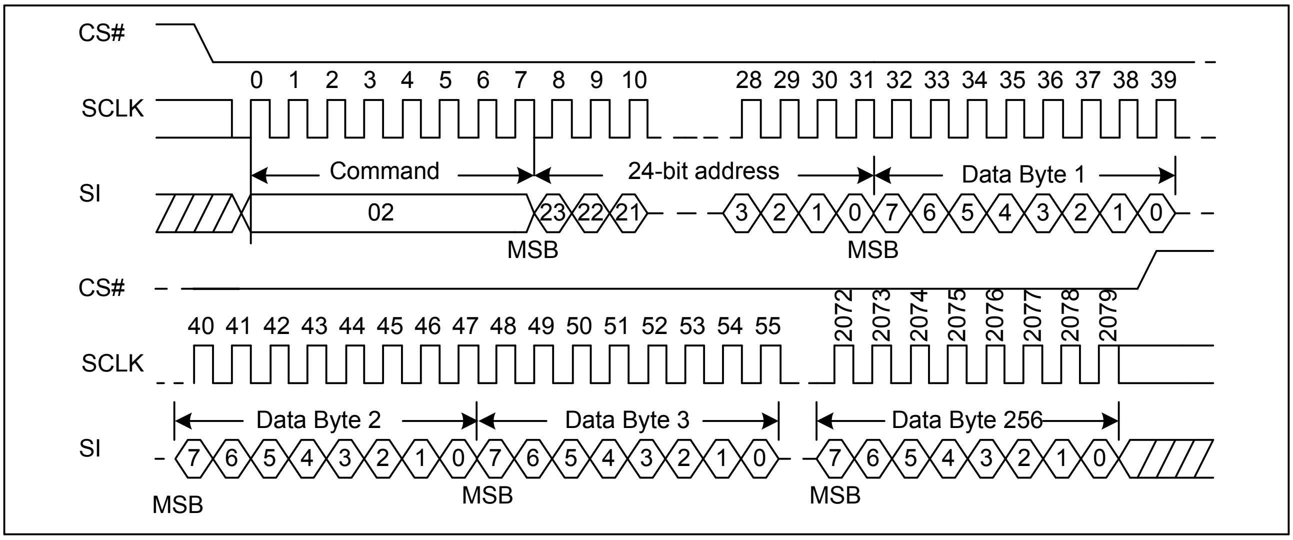
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS # goes high. The command sequence is shown in Figure 10. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP2, BP1, BP0) is not executed.

Figure10. Page Program Sequence Diagram

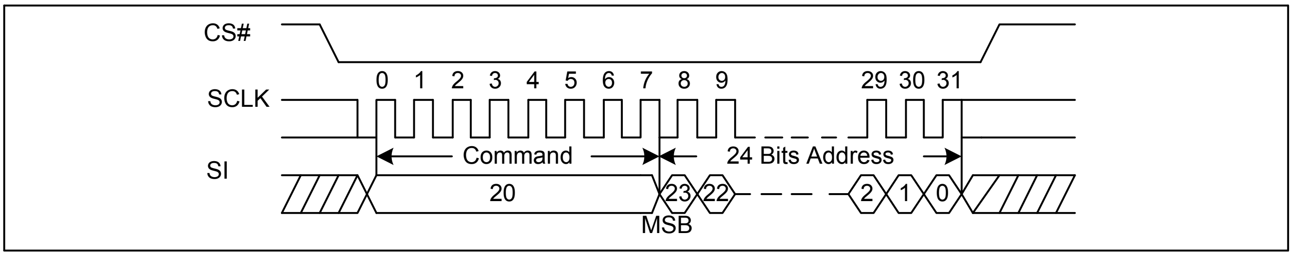


Sector Erase (SE) (20Hex)

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 11. CS# must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bit (see Table 3) is not executed.

Figure11. Sector Erase Sequence Diagram

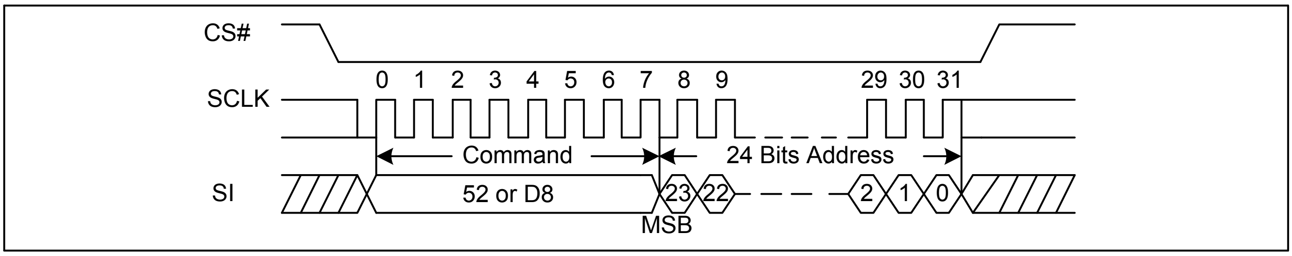


Block Erase (BE) (D8/52Hex)

The Block Erase (BE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The Block Erase command sequence: CS# goes low → sending Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 12. CS# must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{SE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

Figure12. Block Erase Sequence Diagram



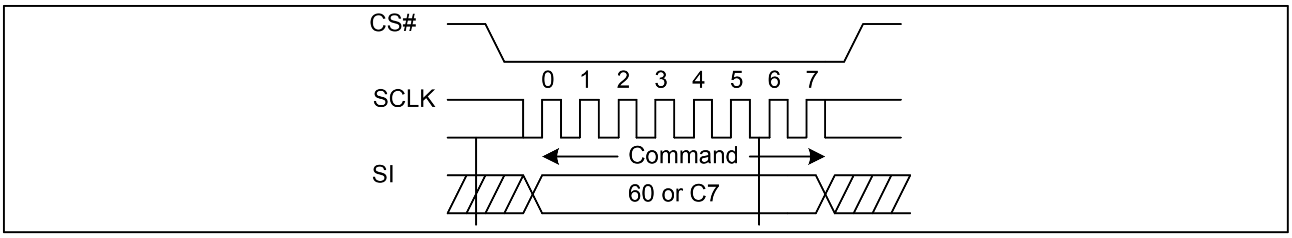
Chip Erase (CE) (60/C7Hex)

The Chip Erase (CE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure 13. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) command is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure13. Chip Erase Sequence Diagram



Deep Power-down (DP) (B9Hex)

Executing the Deep Power-down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Stand-by mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) command. Once the device has entered the Deep Power-down mode, all commands are ignored except the Release from Deep Power-down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Stand-by mode. The Deep Power-down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-down command sequence: CS# goes low → sending Deep Power-down command → CS# goes high. The command sequence is shown in Figure 14 and Figure 15. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Deep Power-down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered. Any Deep Power-down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure14. Deep Power-down Sequence Diagram

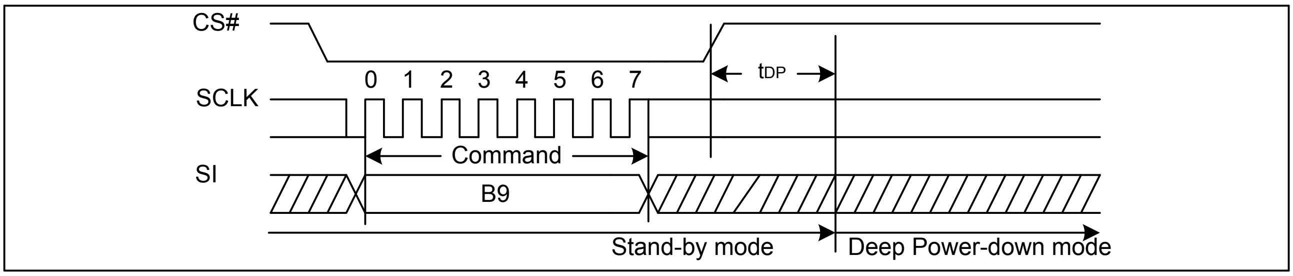
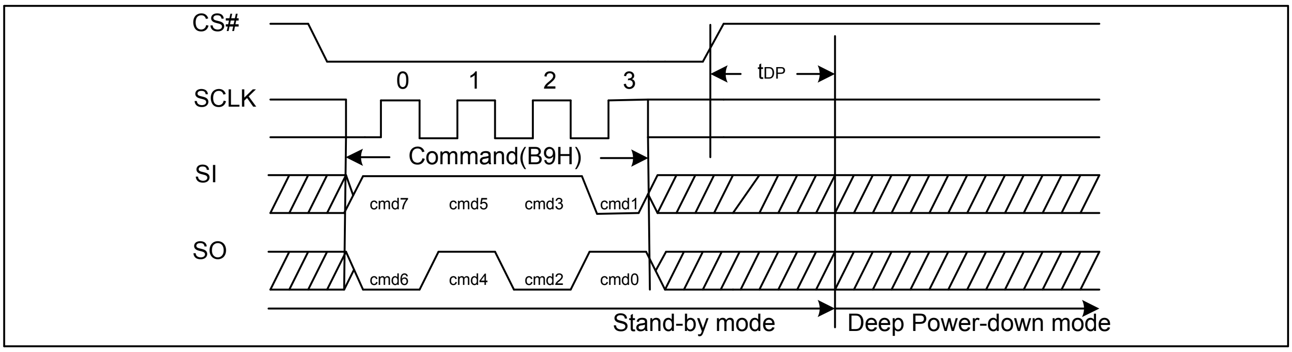


Figure15. Deep Power-down Sequence Diagram of Dual SPI mode



Release from Deep Power-down and Read Device ID (RDI) (ABHex)

When the device has been set Deep Power-down mode, it can ignore all command except the command for release from Deep Power-down and Read Device ID (RDI). The device will be taken out of the Deep Power-down when executing this command.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature which is read by the Read Identifier (RDID) command. The old-style Electronic Signature is supported because of backward compatibility, only, and should not be applied for new designs. JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) command should be used by new design.

When the command is used only to release the device from the power-down state, it is issued by driving the CS# pin low, shifting the command code "ABHex" and driving CS# high as shown in Figure 16 and Figure 16.1. After the time duration of t_{RES1} (See AC Characteristics) the device will recover normal operation and other commands will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When the command is used only to get the Device ID while not in the power-down state, it is initiated by driving the CS# pin low and shifting the command code “ABHex” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 17 and Figure 17.1. The Device ID can be read continuously. The command is completed by driving CS# high.

When CS# is driven high, the device is set in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the device will be transited to the Stand-by Power mode immediately. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2}, and CS# must remain high for at least t_{RES2} (max), as specified. Once under the Stand-by Power mode, the device will wait to be selected, so that it can receive, decode and execute commands. Except when an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) command always provides access to the 8-bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been inputted.

Any Release from Deep Power-down and Read Device ID (RDI) command is not decoded, and has no effect on the cycle that is in progress when an Erase, Program or Write Status Register cycle is in progress,

Figure16. Release Power-down Sequence Diagram

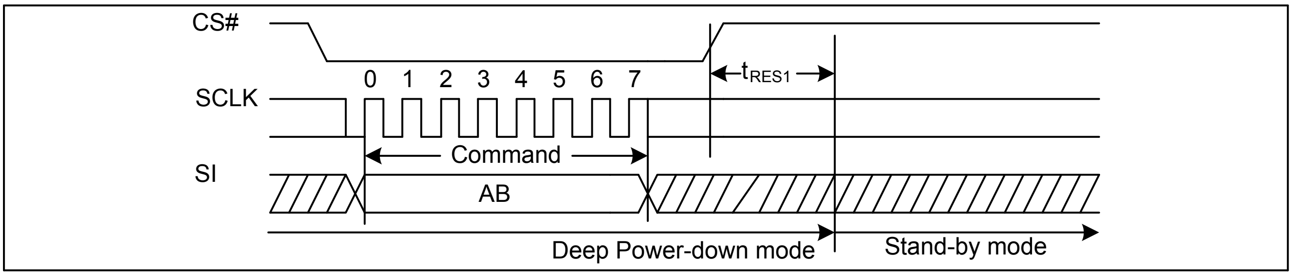


Figure16.1 Release Power-down Sequence Diagram of Dual SPI mode

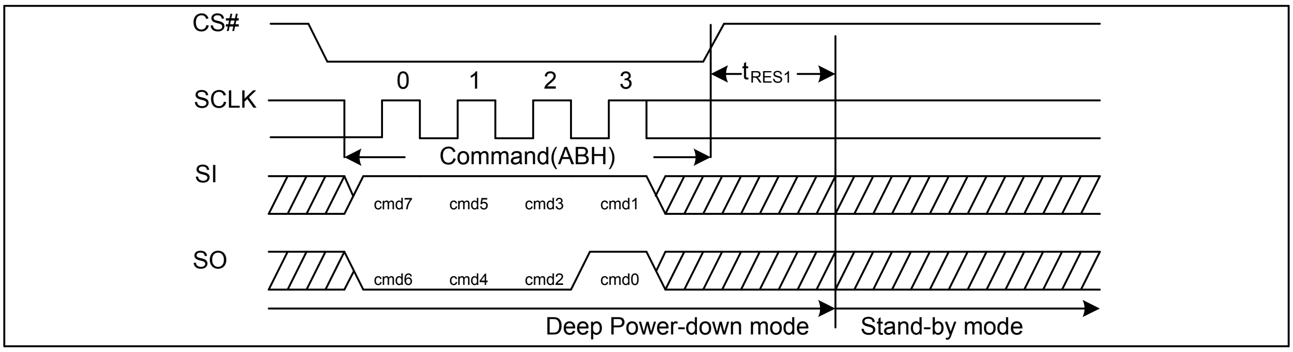


Figure17. Release Power-down/Read Device ID Sequence Diagram

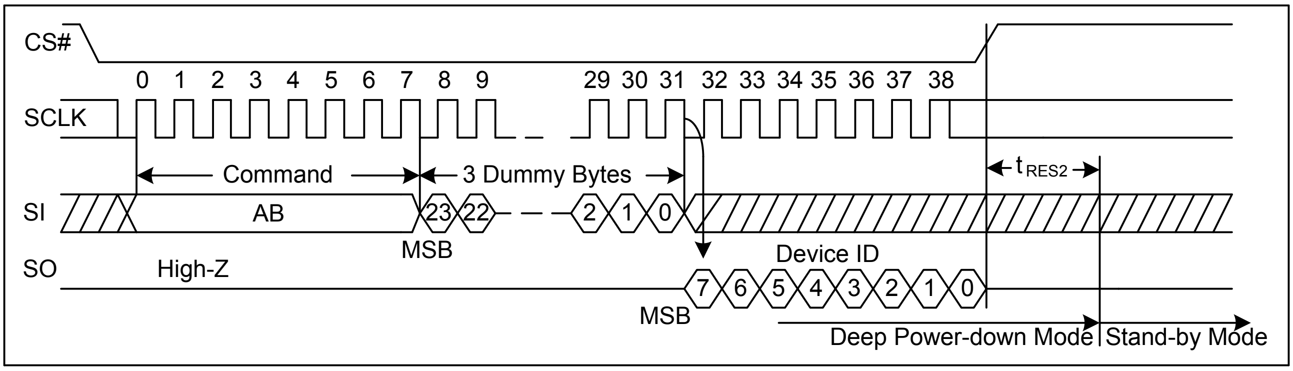
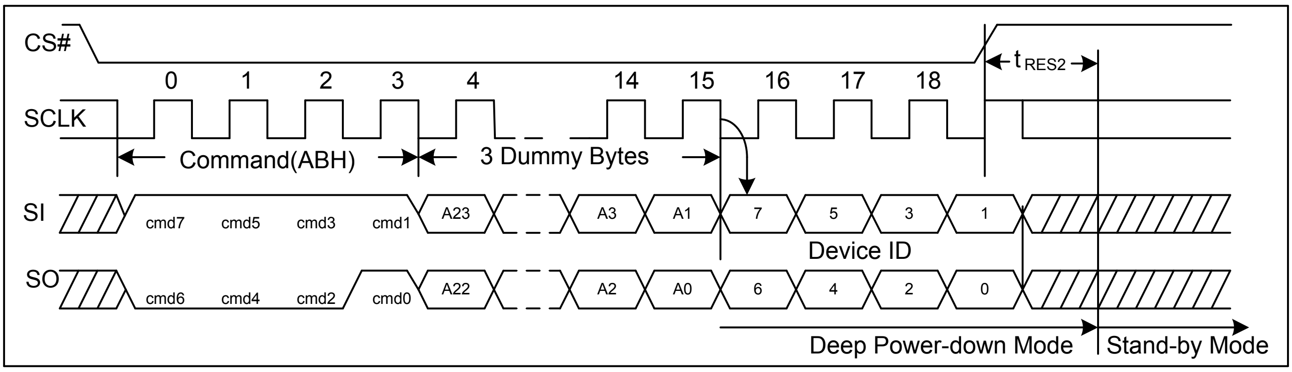


Figure17.1 Release Power-down/Read Device ID Sequence Diagram of Dual SPI mode



Read Manufacture ID/ Device ID (REMS) (90Hex)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-down / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 18 and Figure 18.1. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure18. Read Manufacture ID/ Device ID Sequence Diagram

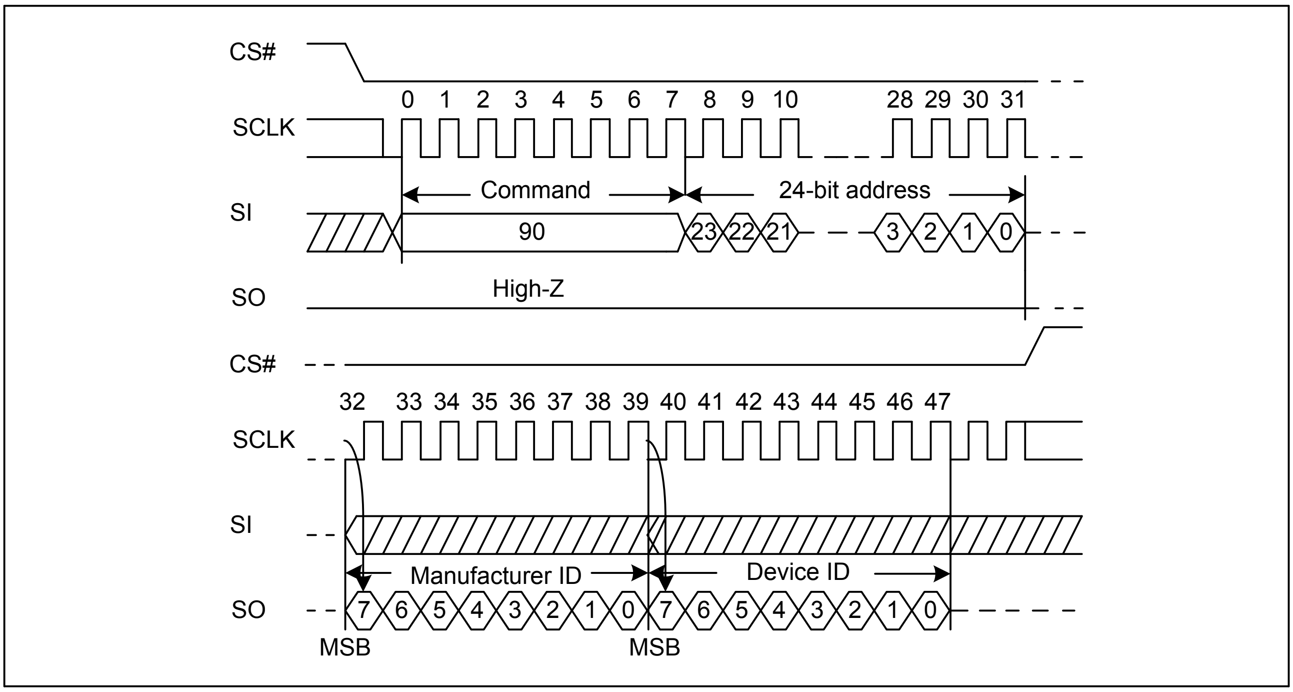
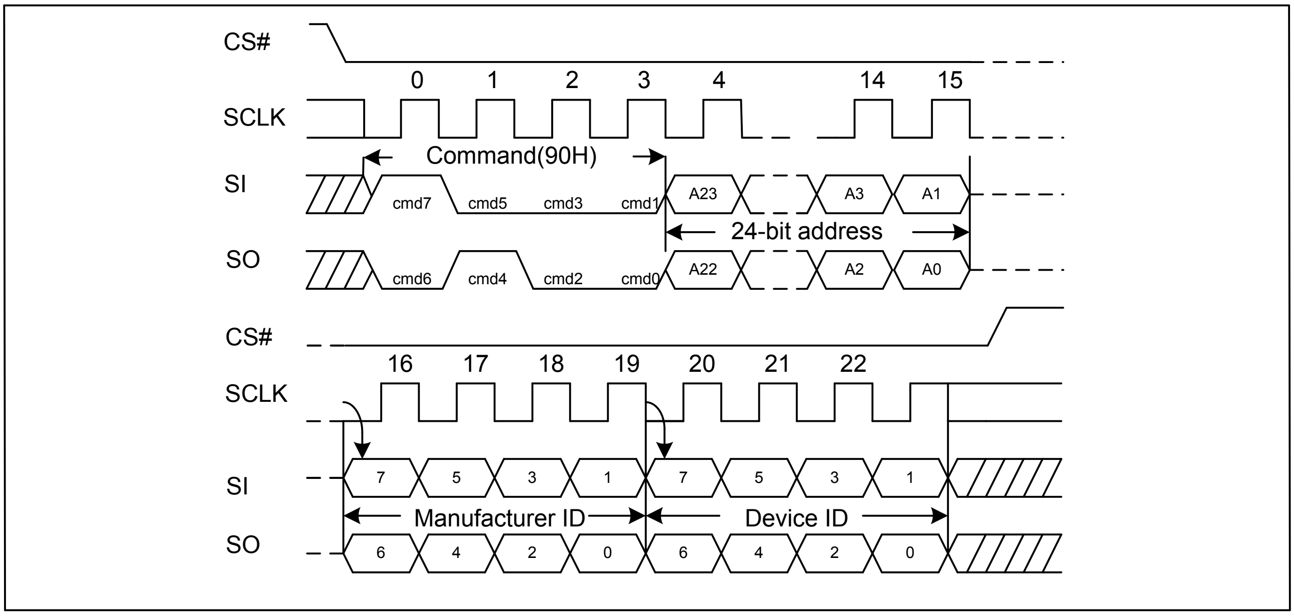


Figure18.1 Read Manufacture ID/ Device ID Sequence Diagram of Dual SPI mode



Read Identification (RDID) (9FHex)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-down mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure 19 and Figure 19.1. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure19. Read Identification ID Sequence Diagram

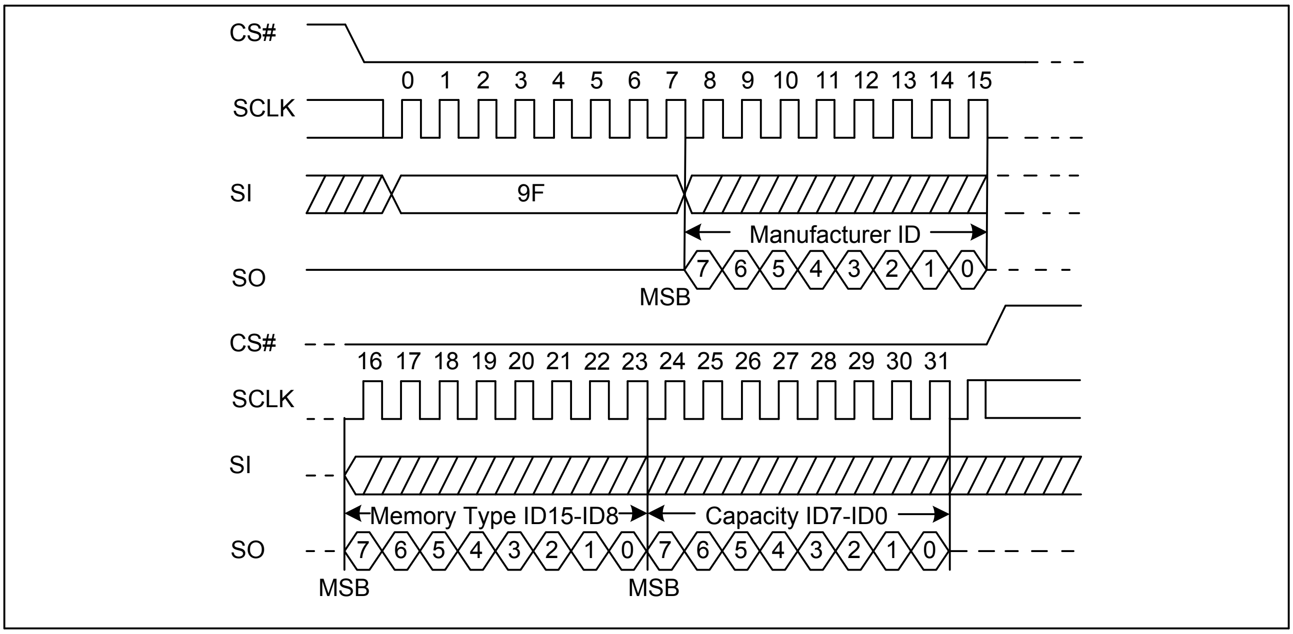
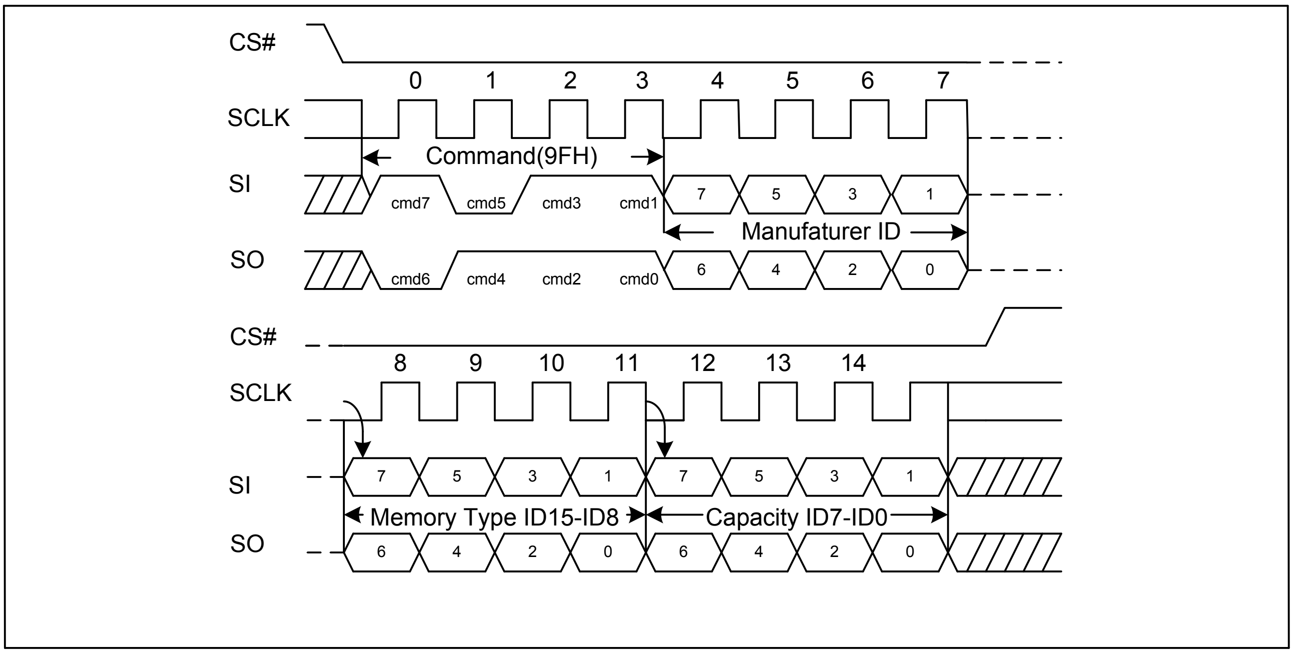


Figure19.1 Read Identification ID Sequence Diagram of Dual SPI mode

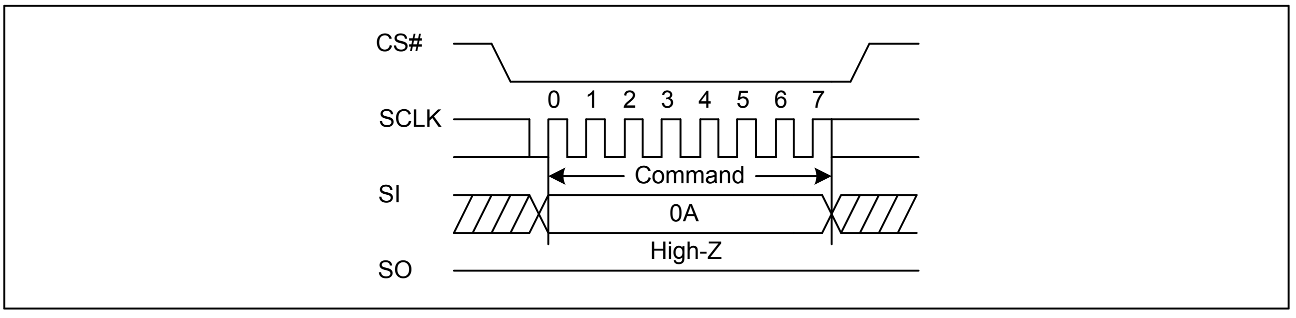


Enter EXT Mode (0AHex)

The device support extend transmission mode to enhance the data throughput. User can use the enter mode commands to switch from normal mode into extend mode and exit by WRDI (04H) command. The Enter EXT Mode command is initiated by executing an 8-bit command 0AH. User can use RDSR command to read the Mode bits from Status Register.

After Power on Reset, the Mode1, Mode0 bits will keep 00, in SPI mode (default mode); After Enter EXT Mode, the Mode1, Mode0 bits will be 01, to Dual SPI mode.

Figure20. Enter EXT Mode Sequence Diagram



Enter OTP Mode (3AHex)

The device has an extra 256 bytes OTP part. User has to input Enter OTP Mode order to enter OTP mode prior to reading/programming or erasing OTP sector. After inputting OTP mode, the OTP part is mapping to part 255, SRP bit becomes OTP_LOCK bit and it can be read by RDSR order. When the clock is '1' the program/erase progress will be disabled. The input data and program LOCK bit to 1 will be ignored by WRSR. After the protect has been cleared user has the right to enter OTP mode. If the OTP sector can only be program and erase when LOCK bit equal '0' and sector 255 not protected. Only sector erase (20H) can erase OTP sector. Under OTP mode, though user can read other sectors, program/erase other sectors only are allowed when OTP_LOCK equal '0'

Figure21. Enter OTP Mode Sequence Diagram

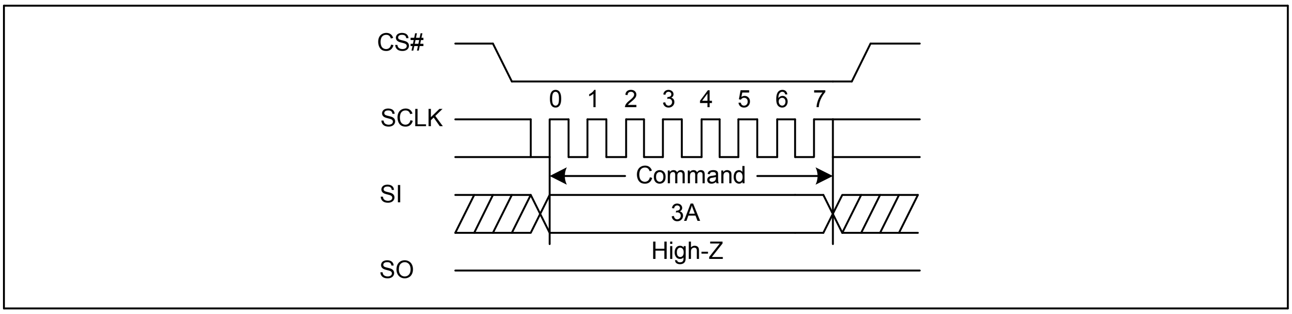
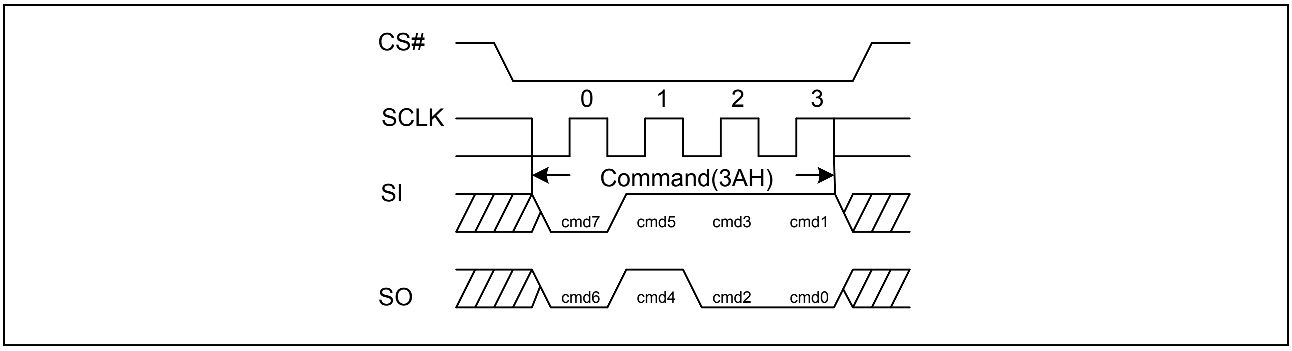


Figure21.1 Enter OTP Mode Sequence Diagram of Dual SPI mode



POWER-ON TIMING

Figure22. Power-on Timing

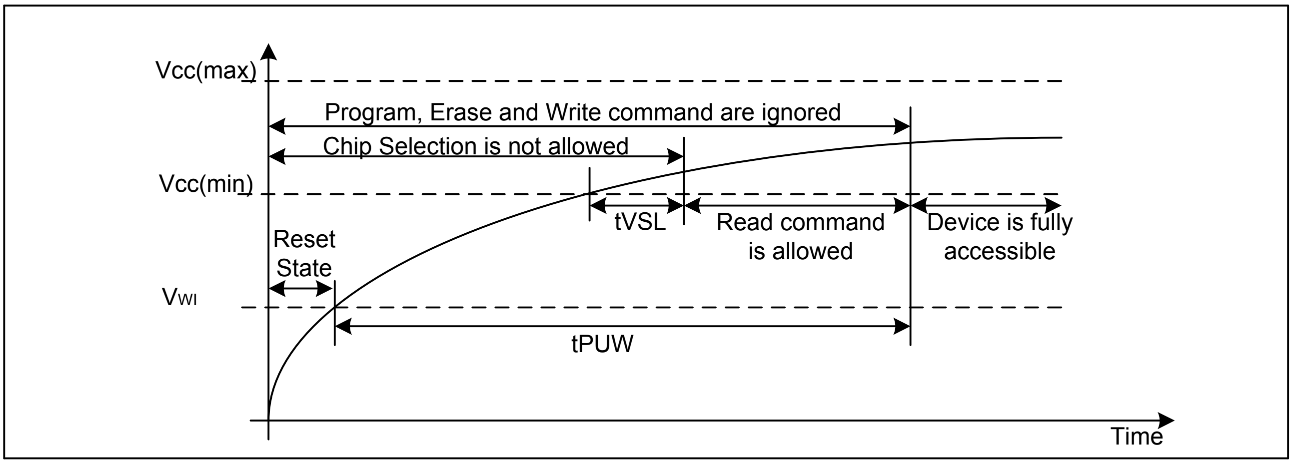


Table5. Power-on Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) to CS# Low	10		us
tPUW	Time Delay from VCC(min) to Write command	1	10	ms
VWI	Write Inhibit Voltage VCC(min)	1	2.5	V

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

DATA RETENTION AND ENDURANCE

Parameter	Test Condition	Min	Units
Minimum Pattern Data Retention Time	150℃	10	Years
	125℃	20	Years
Erase/Program Endurance	-40 to 85℃	100K	Cycles

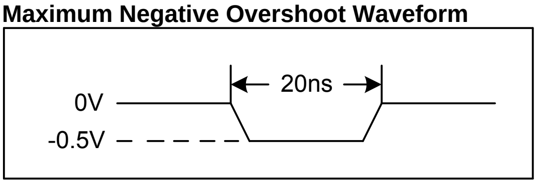
LATCH UP CHARATERISTICS

Parameter	Min	Max
Input Voltage respect to VSS on I/O pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

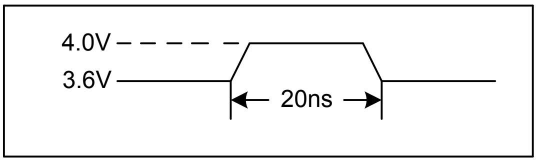
ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Maximum Negative Overshoot Waveform



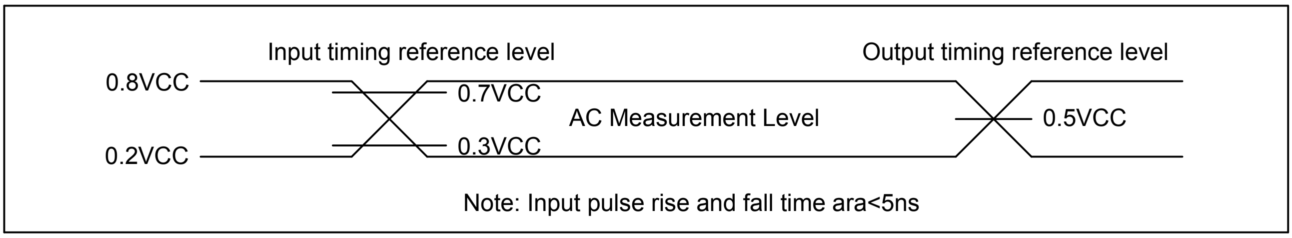
Maximum Positive Overshoot Waveform



CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Tpy	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise and Fall time			5	ns	
	Input Pause Voltage	0.2VCC to 0.8VCC			V	
	Input timing reference Voltage	0.3VCC to 0.7VCC			V	
	Output timing reference Voltage		0.5VCC		V	

Figure23. Input Test Waveform and Measurement Level



DC CHARACTERISTIC

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit.
I_{LI}	Input Leakage Current			±2	μA
I_{LO}	Output Leakage Current			±2	μA
I_{CC1}	Stand-by Current	CS#=VCC, V_{IN}=VCC or VSS		5	μA
I_{CC2}	Deep Power-down Current	CS#=VCC, V_{IN}=VCC or VSS		5	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 150MHz, Q=Open		20	mA
		CLK=0.1VCC / 0.9VCC at 100MHz, Q=Open		18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		15	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC		15	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		15	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		15	mA
V_{IL}	Input Low Voltage		-0.5	0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC	VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2		V

AC CHARACTERISTICS

(T= -40℃~85℃, VCC=2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR	DC.		150	MHz
f_R	Serial Clock Frequency for: Read, RDSR, RDID	DC.		100	MHz
f_T	Serial Clock Frequency In Dual I/O Mode	DC.		100	MHz
t_{CLH}	Serial Clock High Time	3			ns
t_{CLL}	Serial Clock Low Time	3.5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	HOLD # High Setup Time (relative to Clock)	5			ns
t_{CHHL}	HOLD # High Hold Time (relative to Clock)	5			ns
t_{CHHH}	HOLD # Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	HOLD # Low to High-Z Output			3	ns
t_{HHQZ}	HOLD # Low to Low-Z Output			3	ns
t_{CLQV}	Clock Low to Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time after CS# High	100			ns
t_{DP}	CS# High to Deep Power-down Mode			3	μs
t_{RES1}	CS# High to Stand-by Mode without Electronic Signature read			3	μs
t_{RES2}	CS# High to Stand-by Mode with Electronic Signature read			1.8	μs
t_W	Write Status Register Cycle Time		70	120	ms
t_{PP}	Page Programming Time		1.5	5	ms
t_{SE}	Sector Erase Time		0.3	1.2	s
t_{BE}	Block Erase Time		0.8	2	s
t_{CE}	Chip Erase Time		10	20	s

Figure24. Serial Input Timing

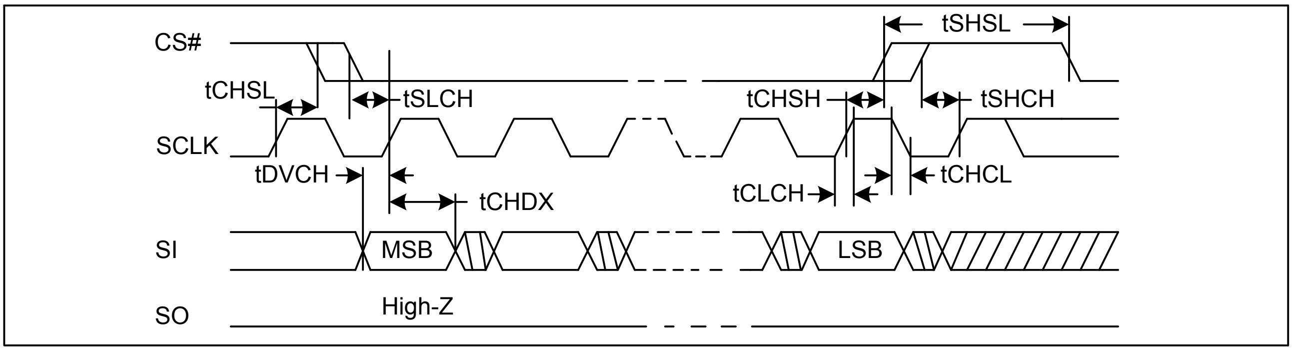


Figure25. Output Timing

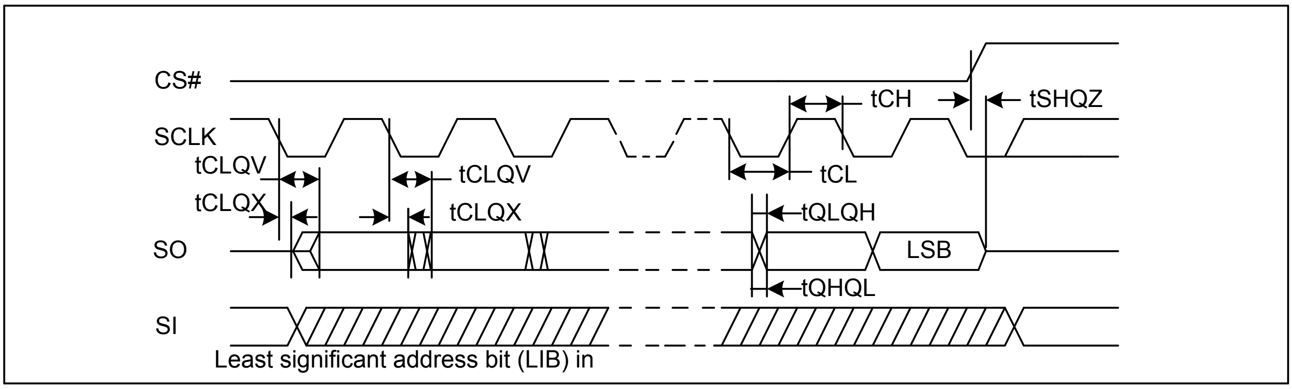


Figure26. Hold Timing

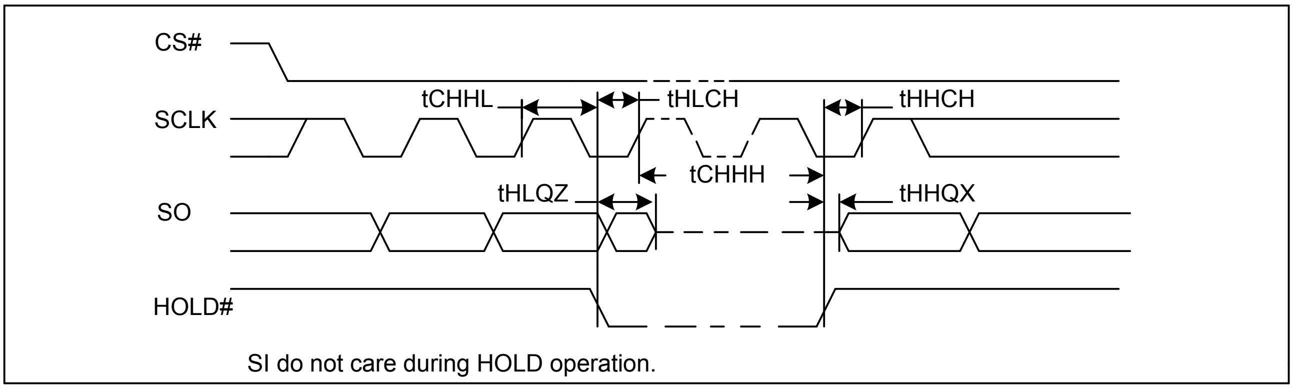
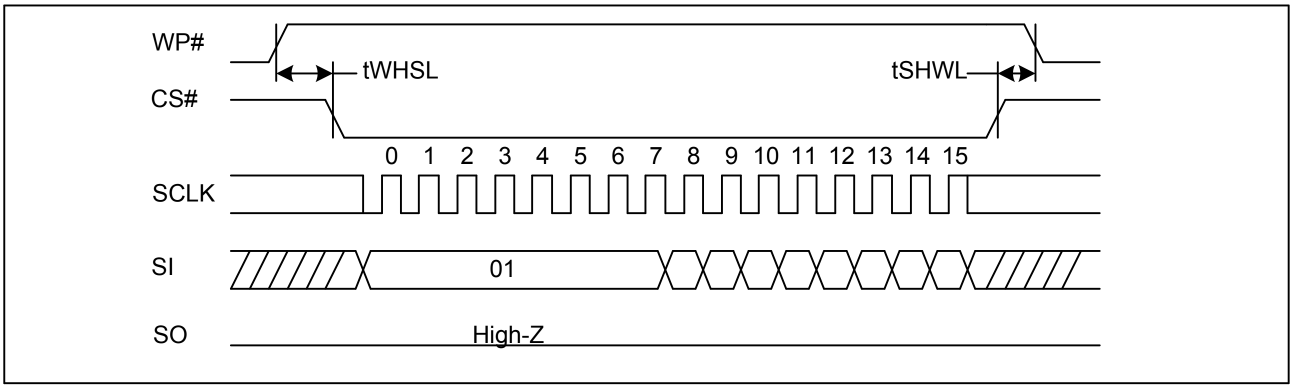


Figure27. WP# Disable Setup and Hold Timing during WRSR when SRWD=1



ORDERING INFORMATION

GD XX X XX X X X X

Packing Type
T:Tube

Green Code
P:Pb Free Only Green Package

Temperature Range
C:Commercial(0℃ to +70℃)
I:Industrial(-40℃ to +85℃)

Package Type
S:SOP8 200mil
P:DIP8

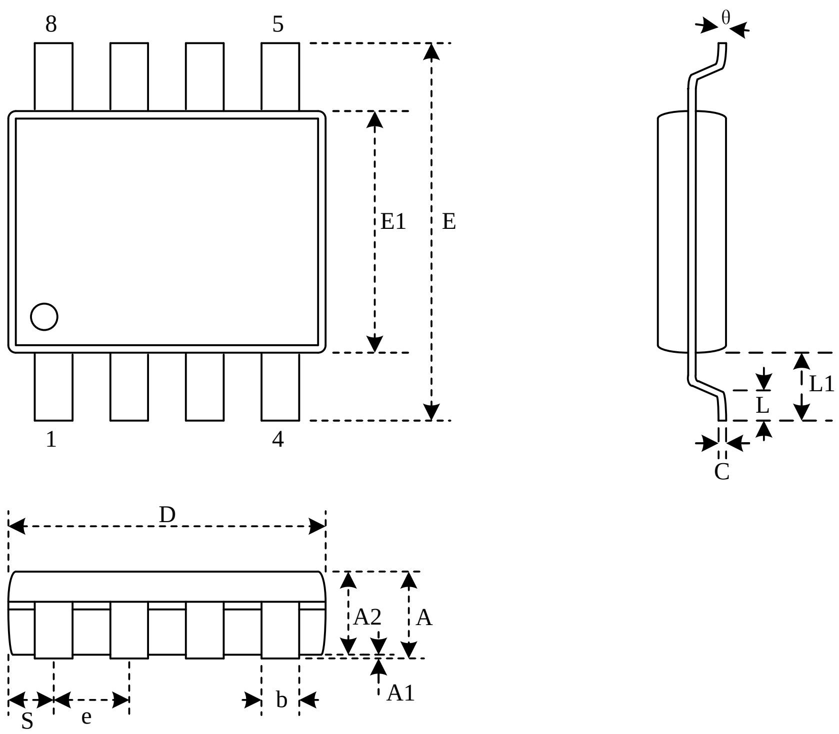
Density
80:8Mb

Series
T:3V,4KB Uniform Sector, Dual Data

Product Family
25:SPI Interface Flash

PACKAGE INFORMATION

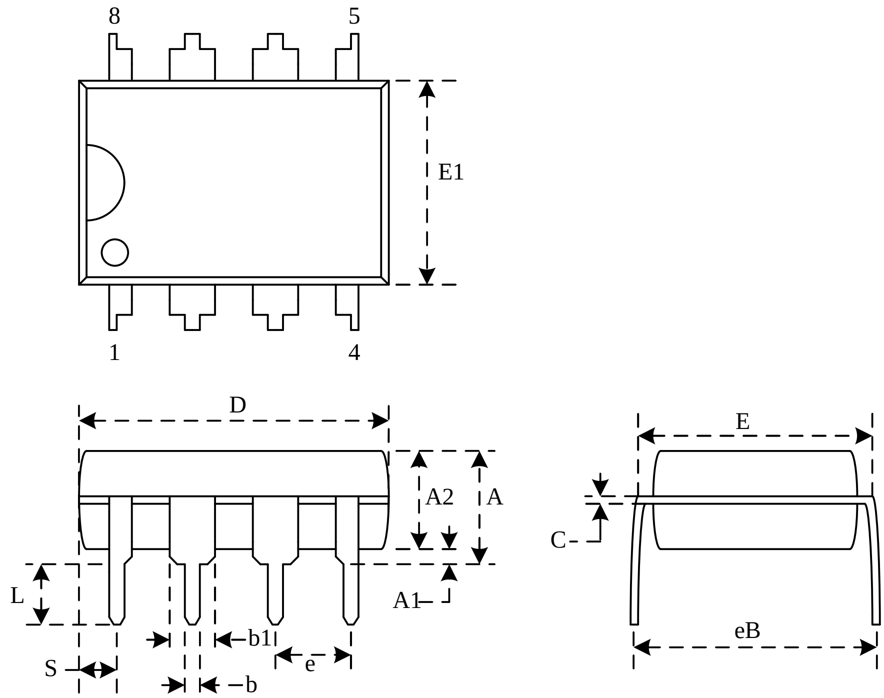
Package SOP8 200MIL



Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min		0.05	1.70	0.36	0.19	5.13	7.70	5.18		0.50	1.21	0.62	0
	Nom		0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.80	1.41	0.88	8
Inch	Min		0.002	0.067	0.014	0.007	0.202	0.303	0.204		0.020	0.048	0.024	0
	Nom		0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.031	0.056	0.035	8

Package DIP8



Dimensions

Symbol / Unit		A	A1	A2	b	b1	C	D	E	E1	e	eB	SL	S
mm	Min		0.38	3.18	0.36	1.14	0.20	9.02	7.62	6.22		7.87	2.92	0.76
	Nom			3.30	0.46	1.52	0.25	9.27	7.87	6.35	2.54	8.89	3.30	1.14
	Max	5.33		3.43	0.56	1.78	0.36	10.16	8.13	6.48		9.53	3.81	1.52
Inch	Min		0.015	0.125	0.014	0.045	0.008	0.355	0.300	0.245		0.310	0.115	0.030
	Nom			0.130	0.018	0.060	0.010	0.365	0.310	0.250	0.10	0.350	0.130	0.045
	Max	0.21		0.135	0.022	0.070	0.014	0.400	0.320	0.255		0.375	0.150	0.060

REVISION HISTORY

Version No	Description	Date
1.0	Initial Release	Apr.25.2008
1.1	Update I_{CC3} Update f_C, f_R Add f_T	Jan.05.2009